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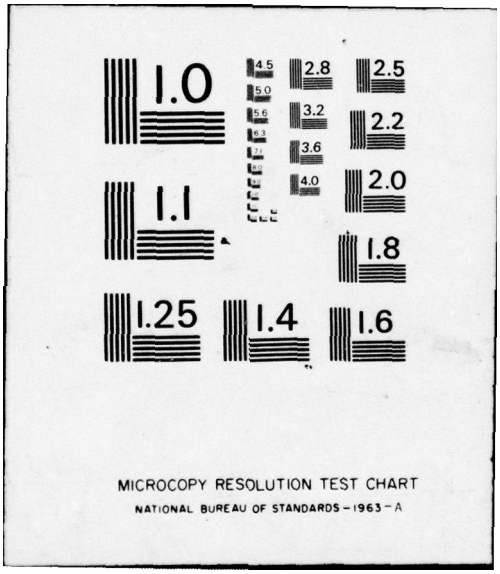
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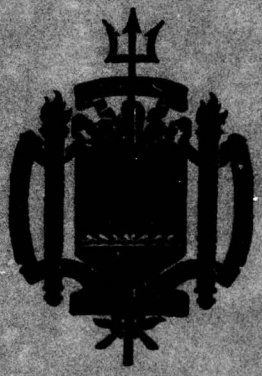
A TRIDENT SCHOLAR PROJECT REPORT

NO. 82

"THE DESIGN OF A SONAR TARGET SIMULATOR"



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ABSTRACT

The design considerations of a device for simulating the motion of passive sonar targets are examined. A specific design is discussed along with its limitations and methods for extending the design to include multiple targets.

False targeting in digital-multibeam-steering (DIMUS) sonars is explored through a simulation. A general method for altering the information in certain display types is developed from the results of the simulation.

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I. Introduction

The purpose of this project is two-fold. First to show that it is possible to realistically simulate motion of passive sonar targets using general purpose micro/minicomputers. This is demonstrated by the design and construction of a device which interfaces a small general purpose minicomputer (a PDP-8/E) and provides an operator with an analog audio signal for practice at detection and manual tracking. The simple design will be further analyzed to point out methods of increasing its capabilities. The second part of this project concerns the simulation of passive sonar targets in the digital-multibeam-steering (DIMUS) sonars. A method will be shown of altering the information flow to standard visual display devices to produce target-like indications, and limitations on hardware implementations will be examined.

II. Analog Simulation

The training scenario requires the simulation of one target moving relative to own ship in a background of noise. The operator was to have only aural detection equipment and a bearing select wheel. The input to the device was to be obtained from two sources, one tape of noise only, and one recording of relatively strong signal-to-noise ratio of the target. Other target information and information about the own ship's maneuvering were to be included to provide

a target moving in bearing and changing SNR.

This concept can be carried to two design extremes. The first is that a small general purpose minicomputer with appropriate input-output devices ought to be able to be programmed to do all of the things required in the problem. The problem can be broken down into one operator input and one output, the other necessary quantities being carried internally. One of the Electrical Engineering Department's PDP-8/E's has sufficient input and output devices (of the proper type) to handle such a program.

The other extreme is the design of a special purpose machine to do all of the computation of target parameters and the simulation of target movement. There are currently devices of this type being produced for the Navy.

The extremes have their disadvantages, and a much more desirable approach can be found somewhere between the two. A general purpose computer has the flexibility to handle any new situation by a small change in programming. This approach involves no new construction, but would dedicate the entire machine to take care of only the simulation. This amounts to buying a micro/minicomputer for a simulator, an expensive solution. Also the amount of time that the machine would have to spend in updating the target solution would seriously hamper the response to the operator's input, even with an elaborate interrupt handling procedure. Since the operator can change his bearing

selection at will and very rapidly, the problems involved in keeping the output signal at the correct level at all times could easily consume more time in the machine than is available. A total hardware design has two drawbacks which make it unsuitable for this project. It is very expensive and very complex, even with the use of large scale integrated circuits.

The compromise is the design of a relatively simple peripheral device to be driven by a small minicomputer. The computer need have nothing more special than a parrallel I/O interface. There are a number of micro/mini-computers available from a variety of sources which might be used for the purpose. Because a PDP-8 was available, the design was tailored to it. But with a little variation in design, the unit could be adapted to an Altair 8800, a Hewlett-Packard 9830, or any other machine of the type.

The design of the unit is a straightforward engineering problem. The operator input is from a V-scan shaft-to-digital (S/D) encoder. This type S/D encoder requires some logic to convert the 25 tracks of information into a 12 bit binary number. The machine input is the twelve bit buffered I/O output register. Only eight of the twelve bits are used for transfer of information, the other bits being used for selecting the registers for storage and timing information.

The rest of the unit takes the difference between

the operators input and the computer's generated target bearing. This quantity is fed into a two's complement true/complement device to obtain the absolute value of that difference (corresponding to the distance off-axis for the sonar array). This number is used as the address to a programmable-read-only-memory (PROM) which contains the gain of the array as a function of the distance off-axis. The output of this first PROM is added to the computer's generated target strength and fed into a second PROM. The second PROM contains the conversion from a logarithmic function (all inputs in dB) to an arithmetic ratio. The ratio is used to control the gain of an amplifier which passes the target signal.

The level control is a multiplying digital-to-analog convertor. The input signal is fed into the device which functions as a digitally controlled variable gain amplifier. A conventional analog summing amplifier is then used to mix the attenuated signal with the background noise. The output is to the operator's listening device, either headphones or a speaker.

In operation the unit receives updated target information (target strength and bearing) from the computer in real time. The computer's real-time clock sets the time interval between new solutions. There are limits on the rate at which the solutions need to be updated. Since the precision of the machine is limited to 12 bits (single

precision), solutions which vary by less than one part in 4000 are meaningless. Internal scaling factors on the computer solution must be set so that they do not show slowly moving targets to be stationary, nor cause large discrete changes in the case of fast moving targets.

There is one other area that the limited precision of the machine bears examination for noticeable effects. The entire scan of the operator is converted into a twelve bit number. The limiting resolution (one bit width) is then .088°. Assuming that a discrete step of more than 0.5 dB would be detectable by the operator, a limit to the narrowest beamwidth which can be simulated can be computed. If the beam pattern is a linear function of bearing, then the half-power points will be at only .5°. Since the value for this limiting case is so far from a realistic value, the effects of a quantized bearing can be ignored.

Although the design is limited to simulation of a single moving target, there are obvious ways to expand the system, and there is a great deal of inherent flexibility. The PROMs that contain the information on the array directivity pattern are easily replaced, and can be programmed for any directivity pattern by merely writing them with the correct values. The computer software determines how the target moves and how strong the signal is. To vary the target strength and to make it and own ship maneuver (for obtaining a bearings only solution to target true

course and speed) it is only a matter of changing the program parameters. To modify the unit to introduce another target, it is only necessary to change the software in the computer and add an identical logic unit in parallel (The operator input section will be shared by both units since it is the same operator looking for two targets.).

This unit has shown that it is possible to construct an inexpensive, yet flexible unit to simulate the motion of a passive sonar target for operator training. Practice in detection and manual tracking can be realistically provided, and depending on the quality and quantity of recorded target signals, practice in classification by quality of sound can be provided.

III. DIMUS Simulation

The second part of this project was to investigate a method by which false targets could be introduced into digital-multibeam-steering (DIMUS) sonars. The concepts of DIMUS sonars were developed during the early 1960's and there are now sonars in use by the Navy based on the DIMUS principles. Conventional techniques for introducing an analog signal at some point in the system are not practical in digital type sonars, and new methods must be developed.

Digital processing of the beams takes each of the analog outputs from the hydrophones and hardlimits them. The process can be thought of as a one bit analog-to-digital (A/D) conversion. The resulting sign information

is then fed into a series of shift registers being clocked at the sampling rate. At appropriately chosen taps on the delay lines, the information is summed across the array. The resulting number represents the instantaneous value of that beam output. By changing the tap points on the delay lines, the array can be "steered" in any direction, just as an analog sonar moves its beam by introducing different delays in the analog delay line and summers (the compensator plates of conventional sonars).

Since there are no mechanical linkages required to accomplish this delay and summing operation, the beam may be moved about without regard for delays or mechanical instabilities encountered with conventional sonars. This results in the ability to "look" in several directions at the same time. This is most noticeable in the digital version of the bearing-time-recorder (BTR), which displays all of its beams simultaneously, as compared to the analog versions which scan all directions in a circular fashion.

In practical designs, the information from the many beams (also called bins) are not available at the same time. In order to conserve the number of interconnecting lines, the data is at some point converted to a series of the sampled bins and transmitted along with identifying information for each bin. Up to this point, the information exists as a quantized time series which represents the bin information and has not been processed for display

purposes.

The numbers which are being transferred are the same as those which would be obtained if an A/D conversion had been done on the analog beam information, plus small non-linear quantization noise and other effects. The underlying assumptions for this linearity are small signal to noise ratio and a large number of elements in the array. The assumptions have been shown to be valid for all cases of practical interest.

Further processing is then required to make use of the information. By performing a digital-to-analog conversion on the numbers, the output can be fed to an aural detection device. The operator moves his search area by selecting which bins are converted. This analog output could be used for spectral analysis, but there are quantization effects which may enter into the problem. The most useful detection and tracking devices are of the BTR type of display. These devices can be of two types, a true RMS (total power) detector, or the rectifying average type detector. Practical designs include the rectifying type detector and a straight time averaging device of several different time lengths. Digital rectifying elements are simpler than a power detection device.

Several authors allude to the simulation of DIMUS sonars on general purpose digital computers. The problem is one which lends itself well to simulation, with the

exception of requiring inordinate amounts of time for small amounts of real time simulated. This was the approach for this part of the project.

The first attempt to simulate a circular array of 48 elements with 108 delay elements per delay line was particularly unsuccessful. Despite the fact that only eleven bins were processed, the program still ran over an hour to simulate only one cycle (about 500 points) of the incoming signal. Since the process depends on the character of the particular noise sample, until a large number of runs could be made, no conclusions could be drawn. Due to the unwieldiness of the program, a new solution had to be found.

The next step was the design of a program which simulated a linear array of 48 elements. Assuming a sinusoidal plane wave coming directly on axis and a Gaussian distributed uncorrelated noise, the program provided information about the character of the bin outputs and the behavior of the rectifying average and RMS detectors. A sufficient number of runs were made of this simulation program to furnish the data from which the conclusions of this paper were drawn.

Since the process is assumed to be linear, and the noise input to the system can be found separately, the signal-only waveform can be recovered from the bin by subtracting the noise-long output. Some non-linear effects were noted in the simulated signals. These were predomi-

nantly noise on the recovered signal not due to the effects of quantization. The nonlinearities were most noticeable at high SNR (0, -5 dB). The other offshoot from the linearity assumption is the ability to insert signal waveforms onto a bin. With the exception of the small nonlinear noise effects a target waveform can be superimposed onto the bin by adding the sampled signal onto each successive bin output. Because of the limited word size, overflow must be accounted for.

Not every application requires aural detection or the use of spectral analysis equipment which would require the entire signal to be present in the digitized bins. The simulation of targets for the BTR displays using rectified average or RMS detectors can use another scheme. As each bin is passed through the interface device, a constant can be added to it if a target signal would be present in that bin. The quantity added to each bin must be an integer because each part of the signal is an integer number. However, it may be necessary to add a non-integer quantity to the average over a long time period. This is accomplished by adding a fixed integer to a fraction of the consecutive bins as chosen at random or according to some other scheme. If the constant to be added to each bin were 3.6, then the integer 4 would be added to 90% of the bins. Several simulation runs were made with this type of tampering, and the results compared the output of the rectifying average type detector to obtain an empirical relationship between

the time average required to simulate a given SNR as measured by the detector.

By analyzing a large number of runs, the effects of the statistical variation can be minimized. The output of the rectifying average detector was calculated for the no-signal and the signal present cases. For low SNR the differences were sometimes negative (that is the signal present case caused a lower deflection than the noise only). However, this fading should be expected as analog devices of the burned paper BTR show the same fading should be present in any realistic simulation.

The relationships between the SNR and the average quantity to be added to the bins is developed further in the appendices.

Speculation on the possible hardware implementation of the scheme for introducing false targets into DIMUS sonars depends strongly on the design of the particular sonar system. Since the U. S. Navy's current versions of these sonars are classified, it is not proper to discuss them here. However, criteria about the devices to accomplish the task are within the scope of this paper.

Assuming that the sonar has a reasonable number of elements (50) and that sampling rates are reasonable for audio work (25 kHz), then a rate for the production of bins in serial form can be assumed to be on the order of 1 MHz. Because the logic will have to examine each bin

word (and a few other parameters about the modifications to be performed) before it changes it, a minimum of four or five instructions will have to be executed between each new word. This fixes a lower limit for a microprocessor clock of 4 or 5 MHz. This is slightly above the limit of present commercially available microprocessors, but will probably be within reason in a short while.

IV. Conclusion

This project has concentrated on two aspects of simulation of sonar targets for training purposes. A new approach to conventional analog simulators was presented, and such a device was constructed. The area of introducing false targets into DIMUS sonars has been explored using large scale general purpose computer simulation of a DIMUS system.

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Remley, Winslow R. "Some Effects of Clipping in Array Processing." The Journal of the Acoustical Society of America, 39, No. 4 (April 1966), 702-707.

Rudnick, Philip. "Small Signal Detection in the DIMUS Array." The Journal of the Acoustical Society of America, 32, No. 7 (July 1960), 871-877.

APPENDIX I

A flow chart of a possible program to run the simulation of moving passive sonar targets on the PDP-8E minicomputer is shown as Figure 1.

Representative portions of the logic design of the interface device for the PDP-8/E and the general layout of the device are given in the following figures. Figure 3 is the logic which decodes the the multi-track shaft-to-digital encoder to a binary number. The logic eliminates the possible ambiquity of all bits not changing at the same and causing false readings near transitions when large numbers of bits are changing, as in the transition from 3 to 4. The output from the lower order bits determine which of two tracks are to be selected for the next bit's output.

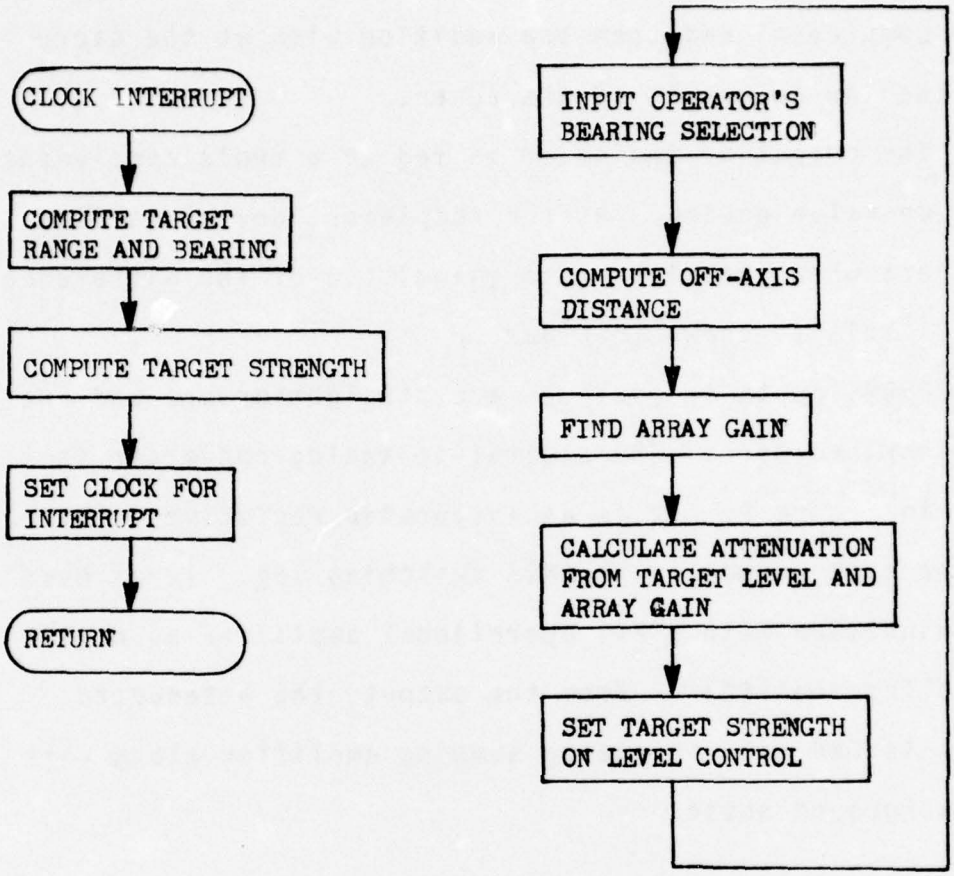
Figure 4 shows the interface logic with the PDP-8's buffered I/O interface. The registers and selection logic are shown for the bearing and target strength inputs. The logic levels from the PDP-8 are negative logic (0 is HIGH, 1 is LOW).

The differencing logic is outlined in Figure 5. A twos's complement subtraction is performed by using the one's complement inherent in the negative logic of the input and forcing a carry into the low order bits of the adder. This is logically equivalent to performing the

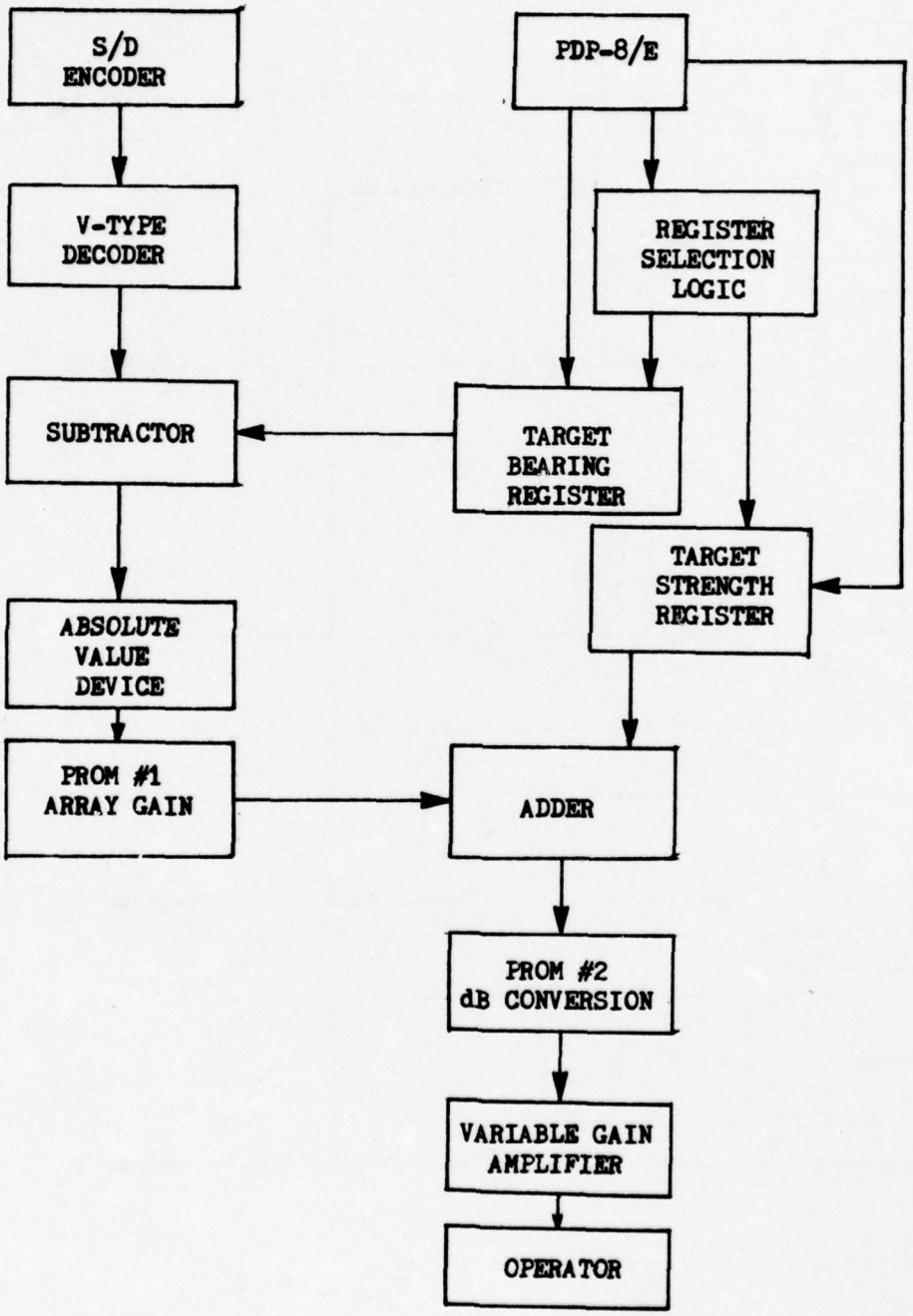
two's complement and then the addition without the carry into the low order bit of the adder.

The output of the adder is fed to a two's complement absolute value device. A true/complement device is used to invert when the high order (sign) bit of the difference is on. This is shown in Figure 6

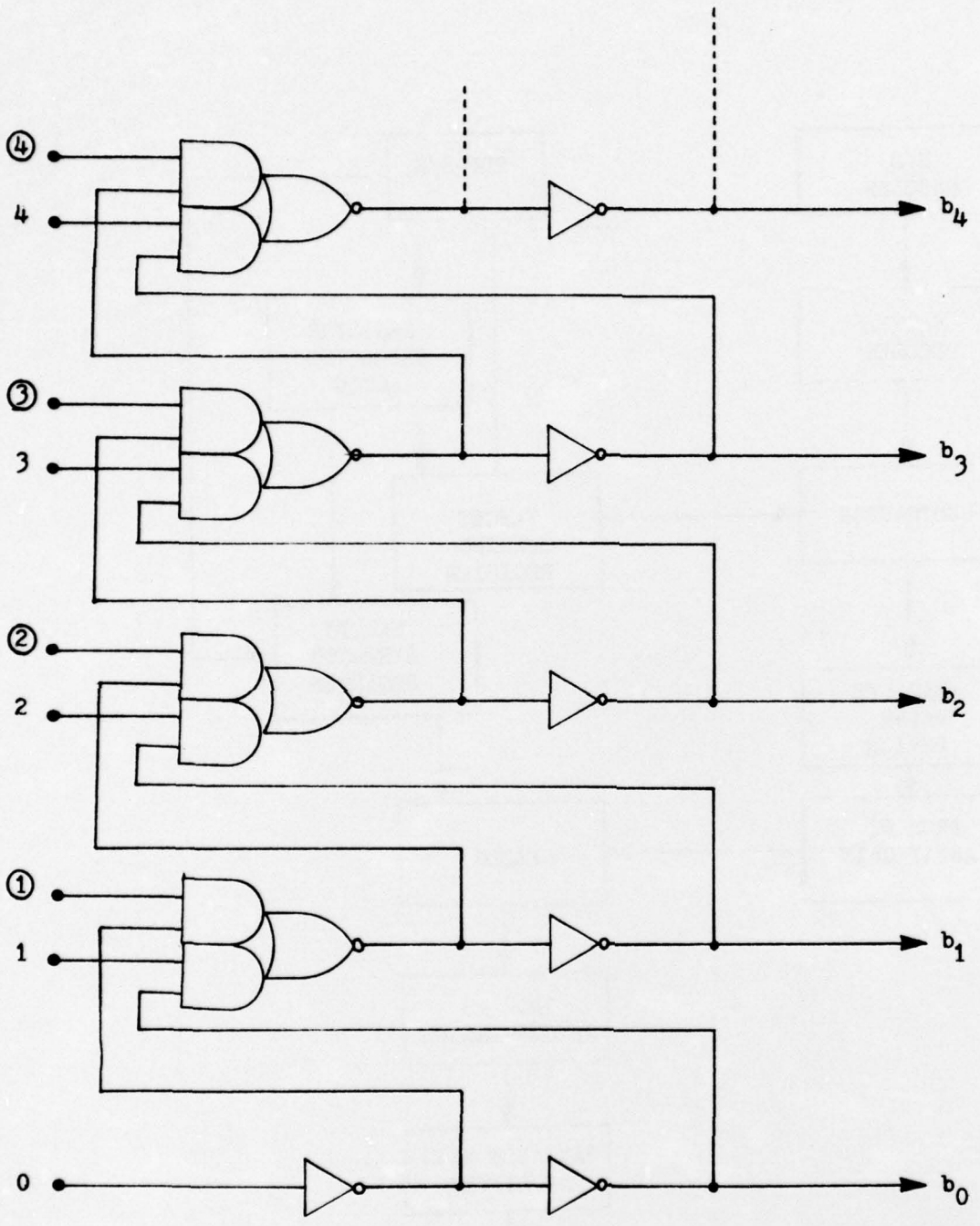
PROM inputs and outputs are straightforward and are not described here. The digital-to-analog converter is shown in Figure 7. It is an integrated resistive voltage divider type network with CMOS switching log. It is used in conjunction with a 741 operational amplifier as a gain controlled amplifier. From the output, the attenuated signal is fed into an analog summing amplifier along with the background noise.



FLOW-CHART FOR SOFTWARE SIMULATION ON PDP-8/E



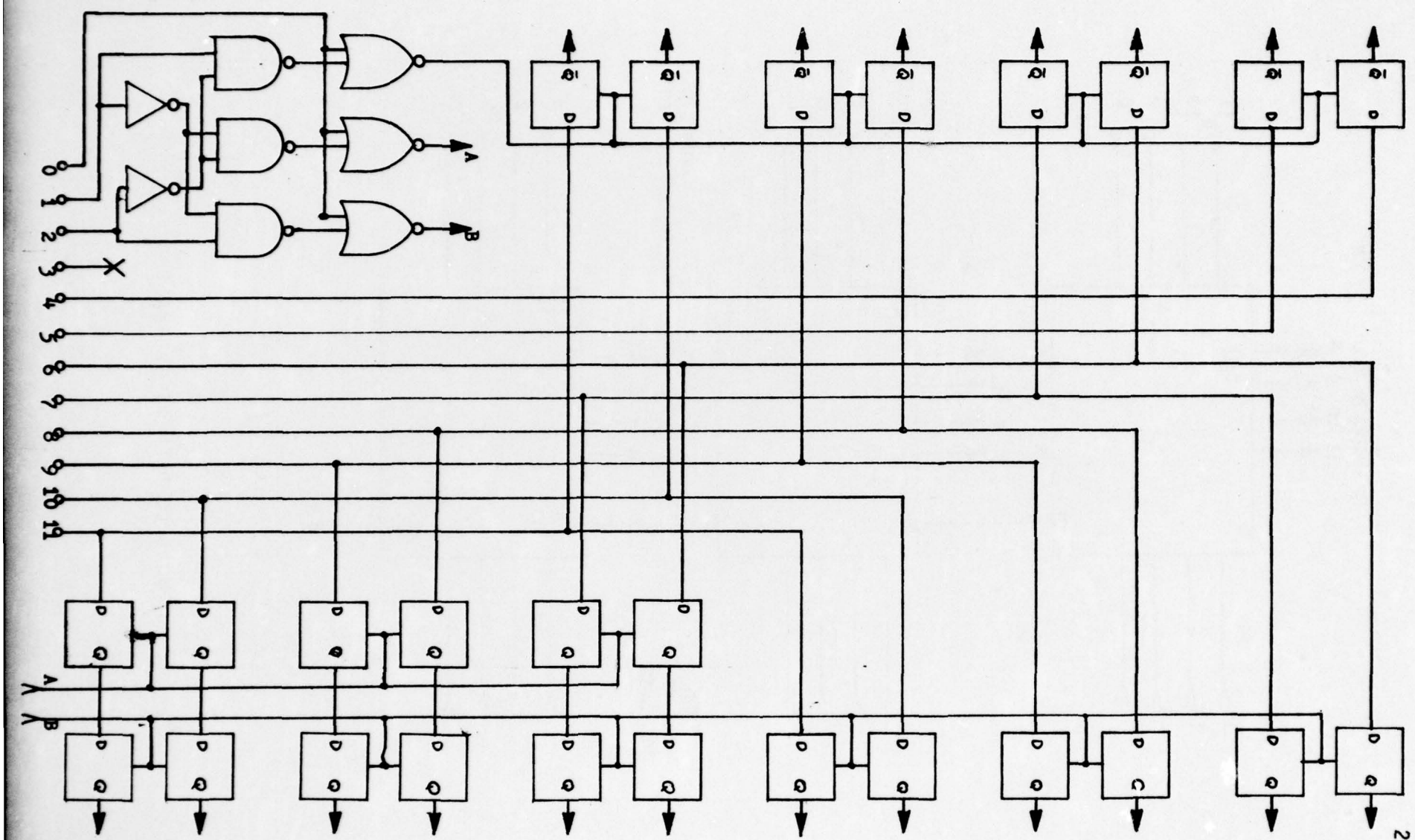
UNCTIONAL DIAGRAM OF SIMULATOR HARDWARE

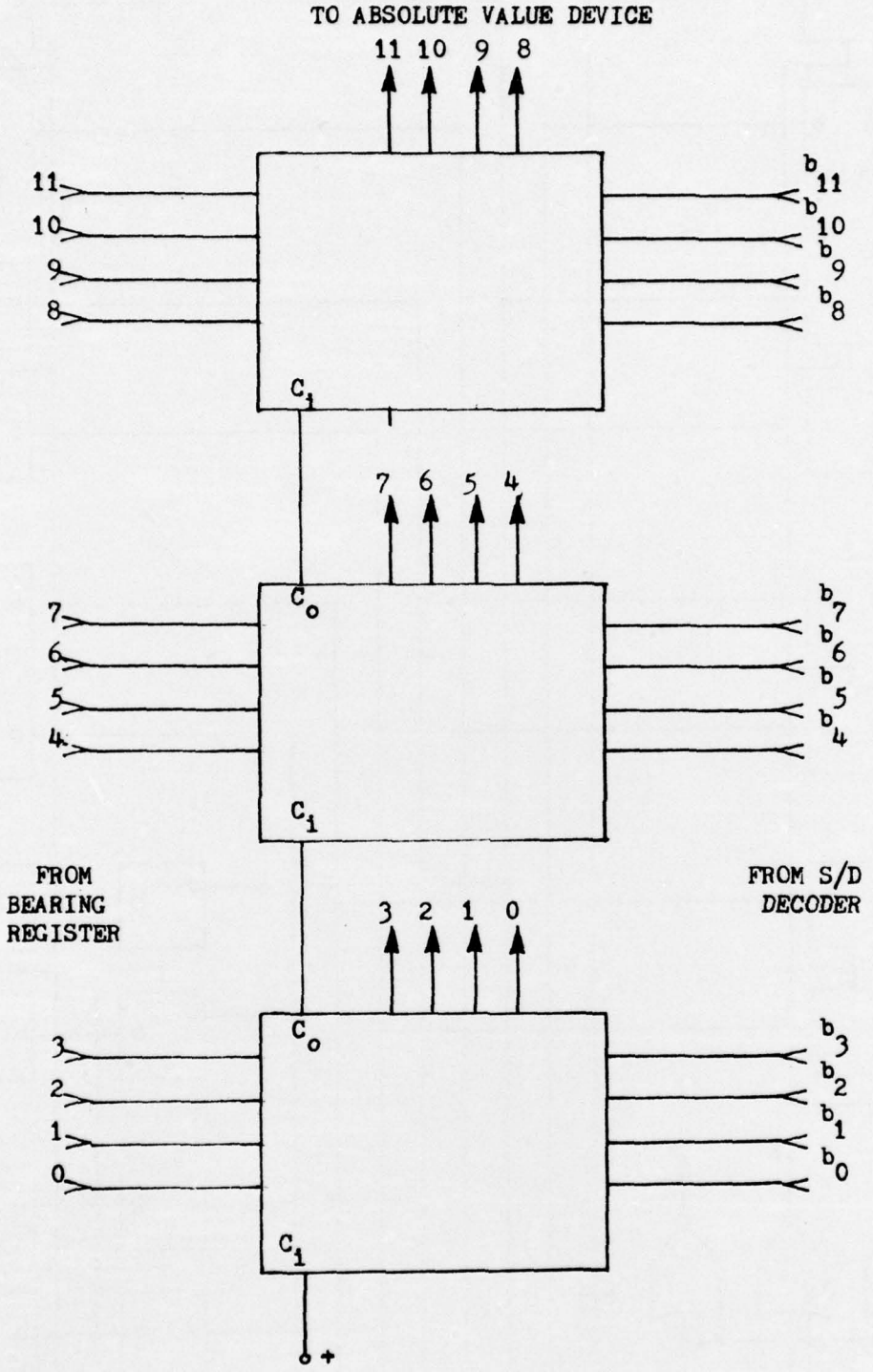


$$b_n = (\overline{b_{n-1}} \cdot \textcircled{n}) + (b_{n-1} \cdot n)$$

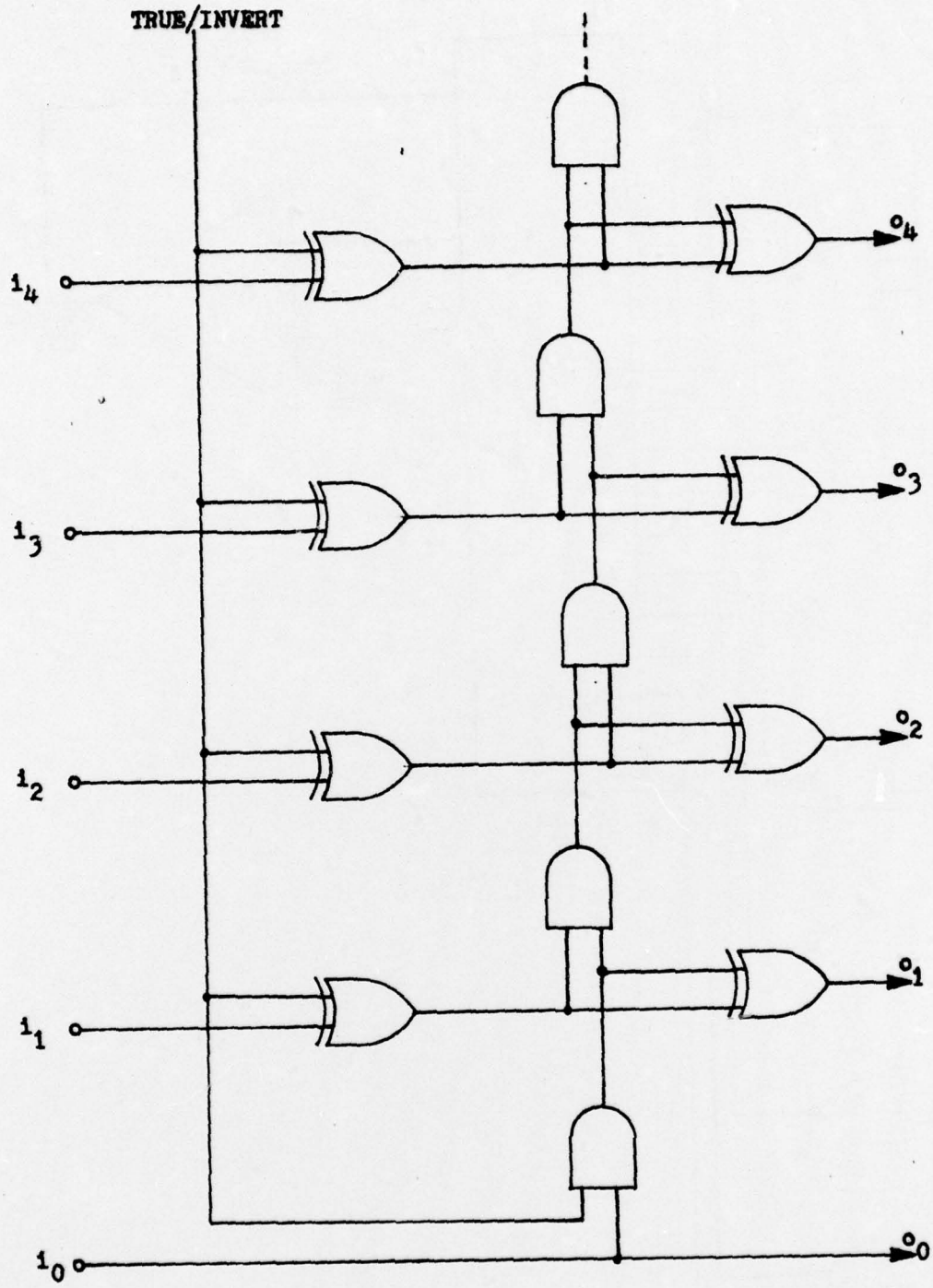
N-TYPE SHAFT-TO-DIGITAL DECODER LOGIC

REGISTERS AND SELECTION LOGIC

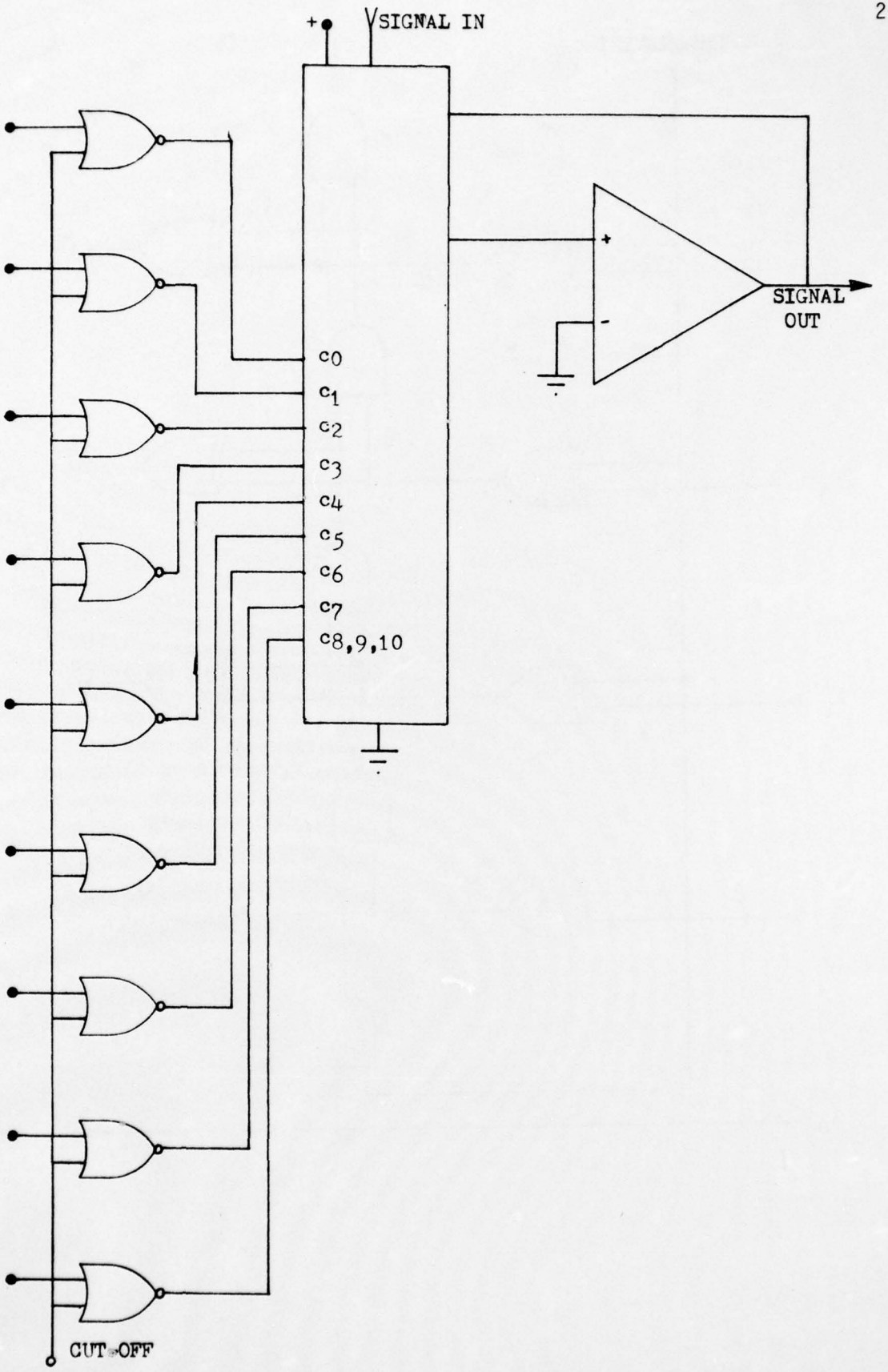




TWO'S COMPLEMENT SUBTRACTOR



ABSOLUTE VALUE LOGIC



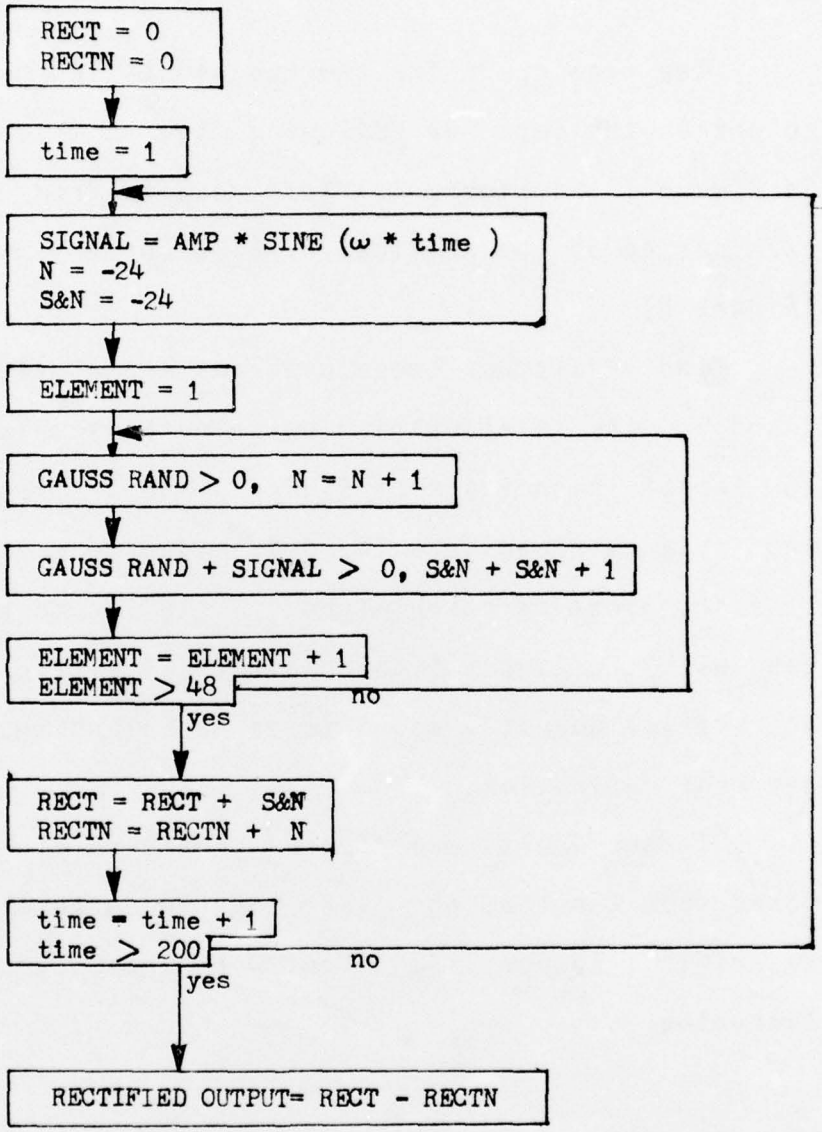
DIGITALLY CONTROLLED VARIABLE GAIN AMPLIFIER

APPENDIX II

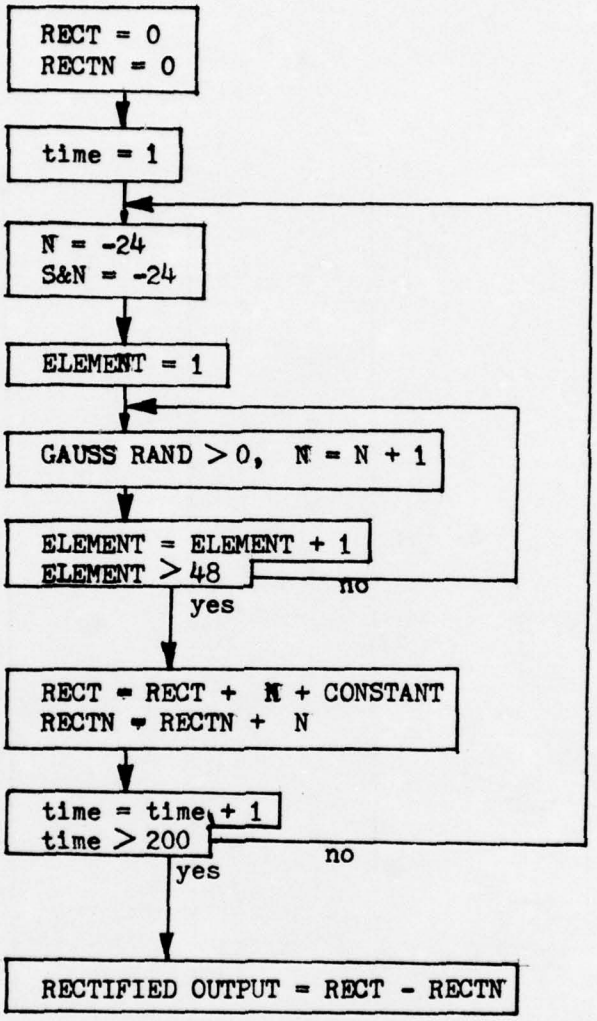
The flow chart for the two simulation programs used to obtain the data for following figures is included here as Figure 1 and Figure 2. This results from direct examination of the physical problem to be simulated (Figure 3).

The results of these programs are plotted as Figures 4 and 5. The relationships between the simulated SNR of the target in the case of Figure 4 and the resulting rectifying average detector deflection were obtained from this graphical representation. A similar technique was used with the Figure 5 to arrive at a relationship between the average quantity added to each bin and the resulting detector deflection.

These results are plotted in Figure 6. It should be noted that the "fading" (variation in detector output) described in paper is inherent with this method of false targeting.

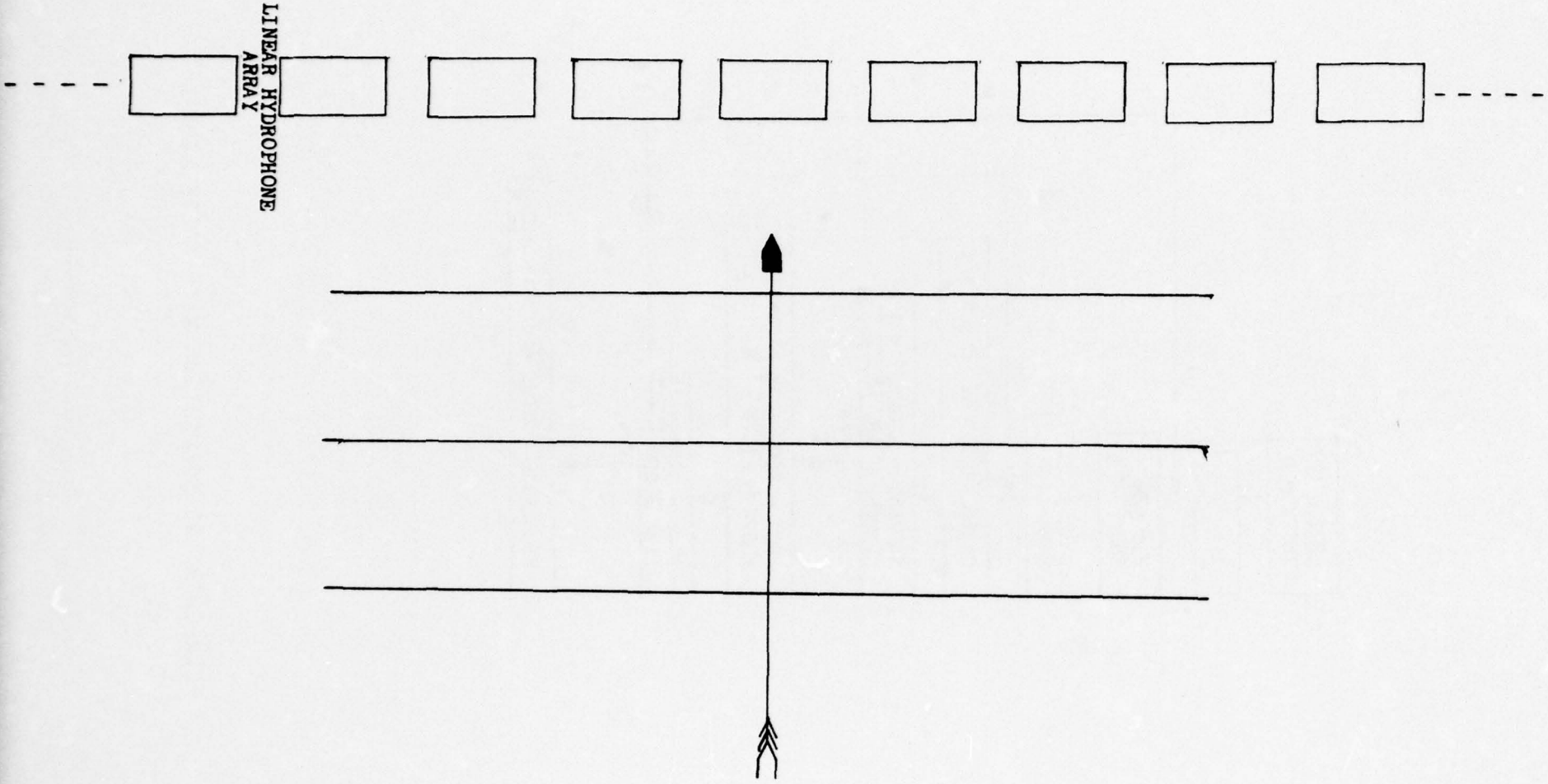


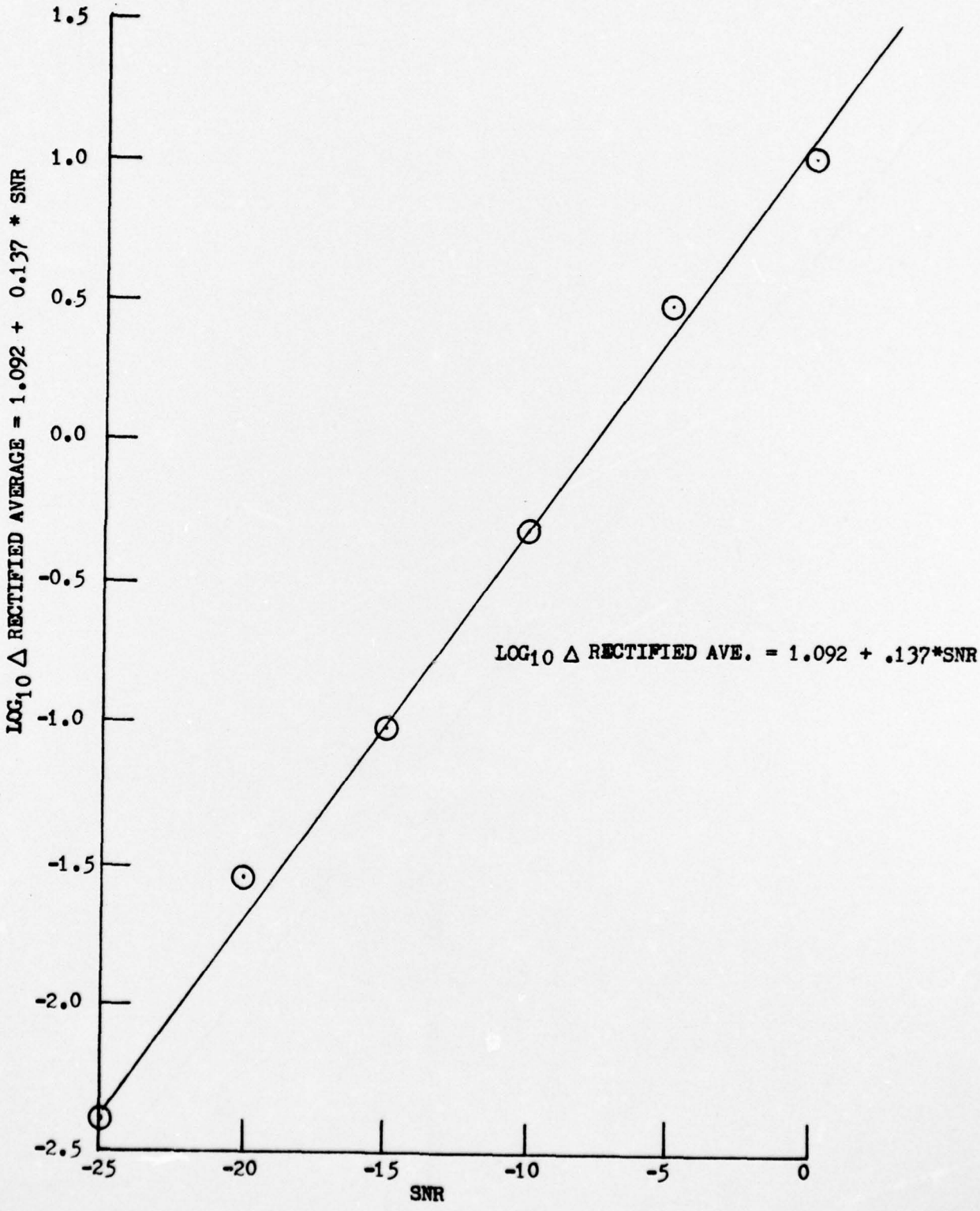
FLOW-CHART OF SIMULATION WITH SIGNAL



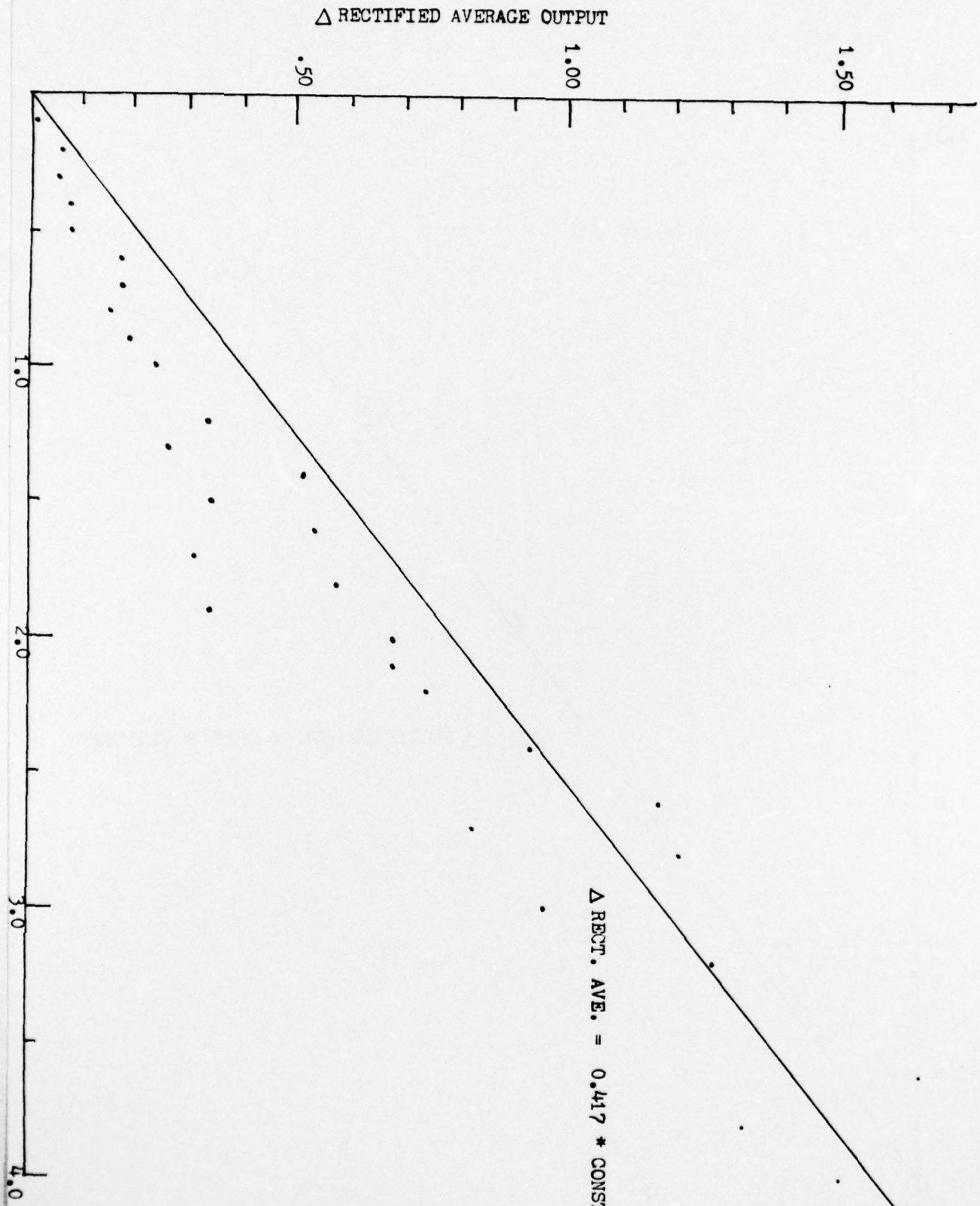
FLOW-CHART OF SIMULATION WITH FALSE SIGNAL

PHYSICAL SITUATION OF SIMULATION





RESULTS OF SIMULATION WITH SIGNAL



RESULT OF SIMULATION WITH FALSE SIGNAL

$$\Delta \text{ RECTIFIED AVERAGE} = 0.417 * \text{CONSTANT} \qquad (1)$$

$$\text{LOG}_{10} \Delta \text{ RECTIFIED AVERAGE} = 1.092 + 0.137 * \text{SNR} \qquad (2)$$

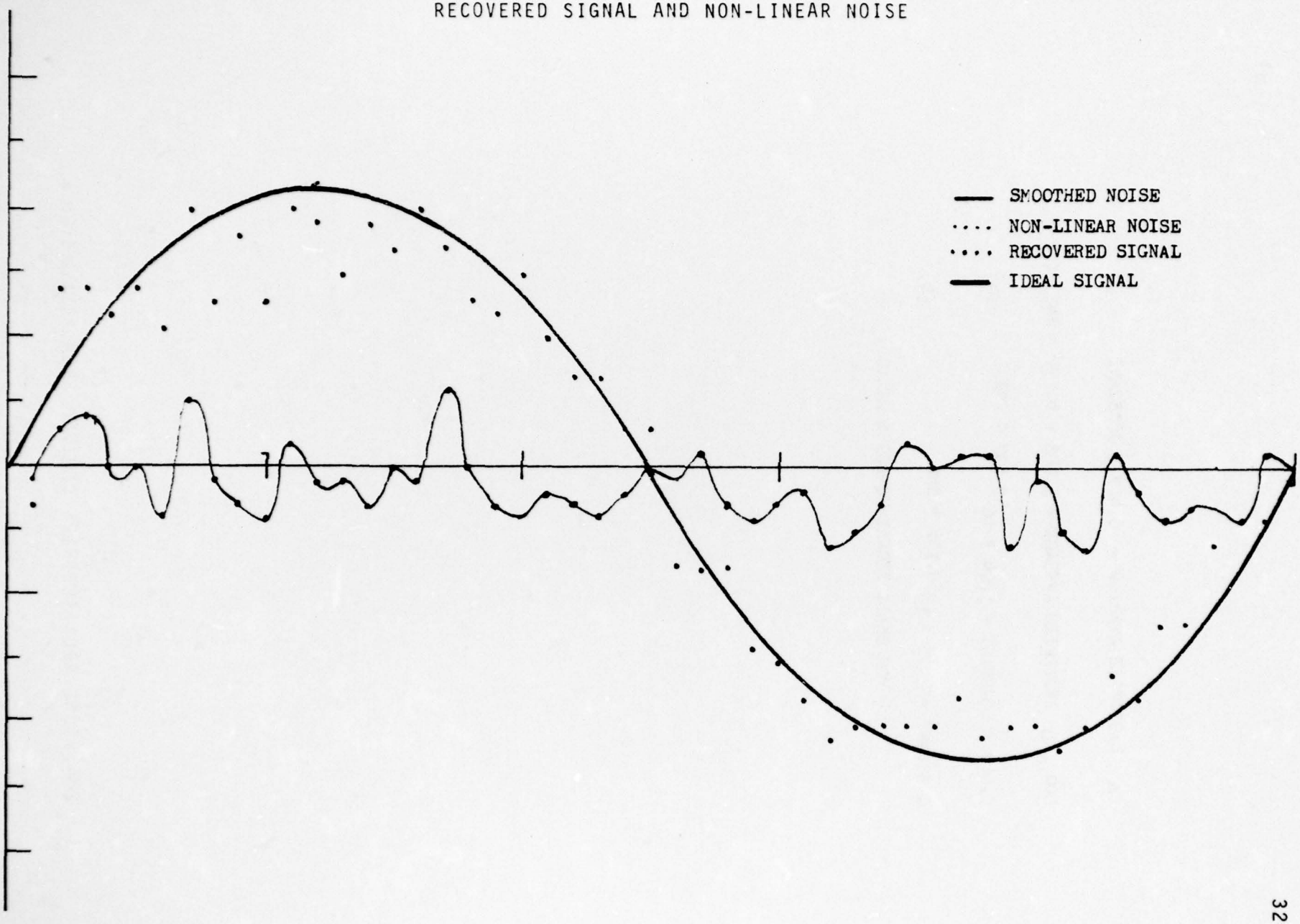
$$0.417 * \text{CONSTANT} = 12.4 * 10^{\,0.137 * \text{SNR}} \qquad (3)$$

$$\text{CONSTANT} = 29.6 * 10^{\,0.137 * \text{SNR}} \qquad (4)$$

(FOR SMALL SIGNAL-TO-NOISE RATIO)

EMPIRICAL RELATIONSHIPS DERIVED FROM SIMULATION

RECOVERED SIGNAL AND NON-LINEAR NOISE



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13. ABSTRACT

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A specific design is discussed in the paper along with its limitations and methods for extending the design to include multiple targets. False targeting in digital-multibeam-steering (DIMUS) sonars is explored through a simulation.

A general method for altering the information in certain display types is developed from the results of the simulation.

Step-by-step flow-charts of the experiments are in the paper.

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